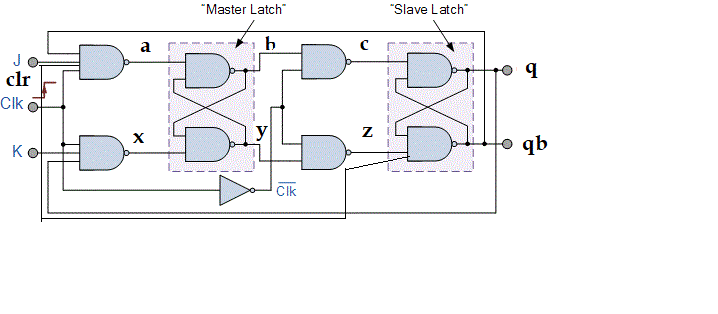
**LAB # 14**

**Objective:** Introduction to xilinx.

**Task1:** Master-Slave j-k Flip Flop in verilog by using Xilinx ISE.

**Circuit diagram:**

**Coding:**

//Design Module

module msjk(q,qb,j,k,clr,clk);

input j,k,clr,clk;

output q,qb;

wire a,b,c,x,y,z,clkb;

assign a=~(j&clk&clr&qb);

assign b=~(a&y);

assign c=~(b&clkb);

assign q=~(c&qb);

assign x=~(clk&k&q);

assign y=~(x&b&clr);

assign z=~(y&clkb);

assign qb=~(z&q&clr);

assign clkb=!clk;

endmodule

//Stimullux Module

module hamza;

reg j,k,clr,clk;

wire q,qb;

msjk f1(q,qb,j,k,clr,clk);

initial

clk=1'b0;

always #5

clk=~clk;

initial

begin

j=1'b0; k=1'b0; clr=1'b0;

#30

j=1'b0; k=1'b1; clr=1'b1;

#30

j=1'b1; k=1'b0; clr=1'b1;

#30

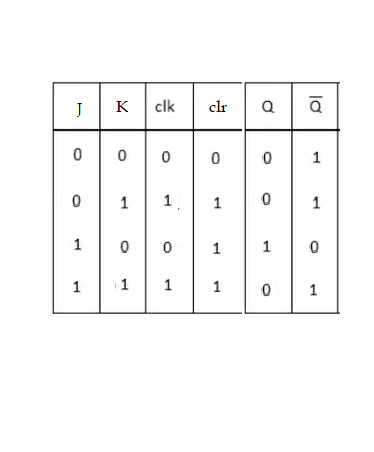
j=1'b1; k=1'b1; clr=1'b1;

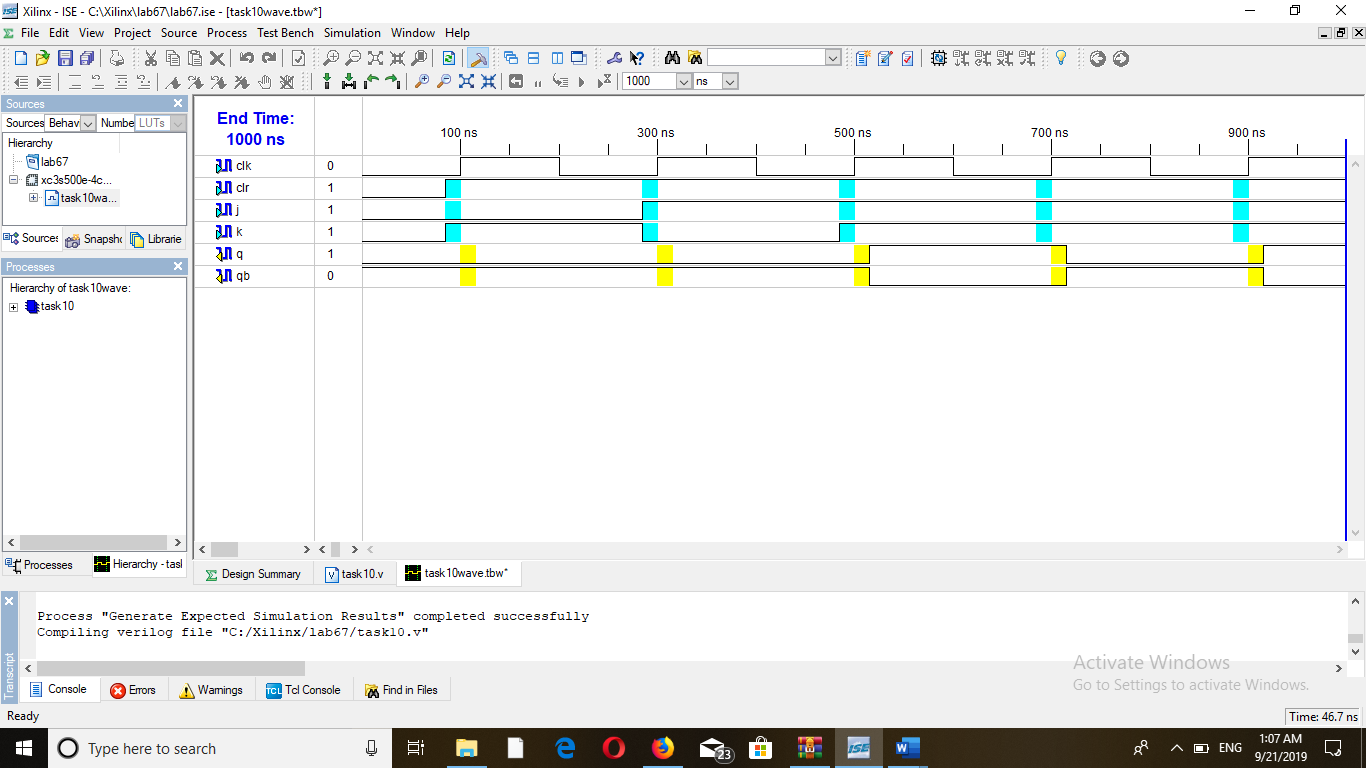
#30

$finish;

end

endmodule

** Truth Table:**

**Results (Timing diagram):**